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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,476	10/24/2001	Koen Lampaert	01CON214P	5455

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EXAMINER	
GARBOWSKI, LEIGH M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 01/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,476	LAMPAERT ET AL.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Miliozzi et al. ["A Design System for RFIC: Challenges and Solutions"].

As per claim 1, Miliozzi et al. disclose a method comprising steps of: receiving a plurality of parameter values for a multi-component circuit having at least one subcircuit model, said plurality of parameter values determining a plurality of parasitic values of said multi-component circuit [Abstract; page 1621, section D., lines 6-17]; generating a layout of said multi-component circuit utilizing said plurality of parameter values, said layout causing said multi-component circuit to have said plurality of parasitic values [page 1618, column A, paragraph 2; pages 1624-1625, section VI.]. As per claim 2 Miliozzi et al. further disclose a step of utilizing said plurality of parasitic values to simulate an electrical behavior of said multi-component circuit prior to said generating step [page 1616, column A, lines 4-9; page 1617, column A, lines 19-22; pages 1626-1627, section VII.]. As per claim 3, Miliozzi et al further disclose wherein said plurality of parameter values comprise a style parameter value [page 1624, section A., lines 6-8]. As per claim 4, Miliozzi et al. further disclose wherein said plurality of parameter values comprises a bulk contact parameter value [page 1620, columns A-B, paragraph 1]. As per claim 5, Miliozzi et al. further disclose wherein each of said plurality of parameter

values is selected from the group consisting of finger width, finger length, number of fingers, current, style, slice and bulk contact parameter values [page 1620, column A, lines 8-12; pages 1624-1625, section VI.]. As per claim 6, Miliozzi et al. further disclose wherein said parasitic values of said at least one subcircuit model comprise a plurality of parasitic resistor and capacitor values [page 1626, column B, lines 2-3]. As per claim 7, Miliozzi et al. further disclose wherein said plurality of parasitic resistor and capacitor values are determined by said plurality of parameter values [page 1616, section III.B.]. As per claim 8, Miliozzi et al. further disclose a step of utilizing said plurality of resistor and capacitor values to simulate an electrical behavior of said multi-component circuit prior to said generating step [page 1616, column A, lines 4-9; page 1617, column A, lines 19-22]. As per claim 9, Miliozzi et al. further disclose wherein said style parameter value determines how interconnect lines are routed in said layout of said multi-component circuit [page 1624, section A., lines 6-8]. As per claim 10, Miliozzi et al. further disclose wherein said bulk contact parameter value determines a location for bulk contacts in said layout of said multi-component circuit [page 1620, columns A-B, paragraph 1].

As per claim 11, Miliozzi et al. disclose a method for designing a circuit block including at least one multi-component circuit, said multi-component circuit having at least one subcircuit model, said method comprising steps of: receiving a plurality of parameter values for said at least once multi-component circuit [page 1616, section A.]; determining a plurality of parasitic values for said at least one multi-component circuit [Abstract; page 1621, section D., lines 6-17]; simulating an electrical behavior of said

circuit block utilizing said plurality of parasitic values [page 1616, column A, lines 4-9; page 1617, column A, lines 19-22; pages 1626-1627, section VII.]; generating a layout of said circuit block including said at least one multi-component circuit, said layout causing said at least one multi-component circuit to have said plurality of parasitic values [page 1618, column A, paragraph 2; pages 1624-1625, section VI.]. As per claim 12, Miliozzi et al. further disclose a step of performing a DRC after said step of generating said layout [page 1618, column A, paragraph 3, lines 1-4]. As per claim 13, Miliozzi et al. further disclose a step of performing a LVS verification after said step of generating said layout [page 1618, column A, paragraph 3, lines 4-5]. As per claim 14, Miliozzi et al. further disclose a step of extracting parasitic parasitics after said step of generating said layout [page 1618, column A, paragraph 3, lines 5-6]. As per claim 15, Miliozzi et al. further disclose wherein said plurality of parameter values comprise a style parameter [[page 1624, section A., lines 6-8]. As per claim 16, Miliozzi et al. further disclose wherein said plurality of parameter values comprises a bulk contact parameter value [page 1620, columns A-B, paragraph 1]. As per claim 17, Miliozzi et al. further disclose wherein each of said plurality of parameter values is selected from the group consisting of finger width, finger length, number of fingers, current, style, slice and bulk contact parameter values [page 1620, column A, lines 8-12; pages 1624-1625, section VI.]. As per claim 18, Miliozzi et al. further disclose wherein said parasitic values of said at least one subcircuit model comprise a plurality of parasitic resistor and capacitor values [page 1626, column B, lines 2-3]. As per claim 19, Miliozzi et al. further disclose wherein said plurality of parasitic resistor and capacitor values are

determined by said plurality of parameter values [page 1616, section III.B.]. As per claim 20, Miliozzi et al. further disclose a step of utilizing said plurality of resistor and capacitor values to simulate an electrical behavior of said multi-component circuit prior to said generating step [page 1616, column A, lines 4-9; page 1617, column A, lines 19-22]. As per claim 21, Miliozzi et al. further disclose wherein said style parameter value determines how interconnect lines are routed in said layout of said multi-component circuit [page 1624, section A., lines 6-8]. As per claim 22, Miliozzi et al. further disclose wherein said bulk contact parameter value determines a location for bulk contacts in said layout of said multi-component circuit [page 1620, columns A-B, paragraph 1].

As per claims 23-34, Miliozzi et al. disclose a system comprising a computer for implementing the methods as outlined above [Abstract].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Charbon et al. disclose "Generalized Constraint Generation for Analog Circuit Design." Ferrario et al. disclose "Moving from Mixed Signal to RF Test Hardware Development." Jones et al. [U.S. Patent #5,666,288] disclose designing an IC. O'Riordan et al. [U.S. Patent #6,381,563 B1] disclose generating circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2800.

LEIGH M. GARBOWSKI
PRIMARY EXAMINER